29. (new) A method according to claim 28, wherein the first and second recessed sections each include sidewalls and a lower surface, the method further comprising forming a protective layer covering the sidewalls and the lower surface of the substrate in the first and second recessed sections prior to the implanting an impurity.

(P6 Cont'd)

30. (new) A method according to claim 6, wherein the first semi-recessed LOCOS layer is positioned between and in contact with the source region and the gate dielectric layer, and the second semi-recessed LOCOS layer is positioned between and in contact with the drain region and the gate dielectric layer, and wherein the implanting is controlled so that the first and second offset impurity layers are formed to each include a side portion that extends along a lower surface of the gate dielectric layer.--

Remarks

This amendment is in response to the Office Action dated August 14, 2002. Claims 6, 9, 14 and 16 have been amended and new claims 21-30 have been added. Claims 6-16 and 21-30 are currently pending. Reexamination and reconsideration are respectfully requested.

Applicant amended the specification by inserting the application number for application docket number 15.42/5850 into the specification at page 1.

Claim 6 was amended to insert a semicolon ";" after the word "formed" at the end of line 10. This amendment is being made for clarity and not in response to any rejection.

Claim 14 was rejected under 35 U.S.C. 112, second paragraph as indefinite. Applicant has amended the claim to insert the term "and" between the terms "greater" and "less". Applicant respectfully submits that claim 14 complies with section 112.

Claims 6-8 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,181,090 to Maruo in combination with U.S. Patent No. 5,946,577 to Tanaka. The rejection is respectfully traversed.

Applicant respectfully submits that one of ordinary skill would not make the combination of Maruo and Tanaka suggested by the Examiner. Applicant notes that Tanaka appears to teach etching the surface of a substrate to form a groove and then forming an enhanced oxide film.

(Tanaka at col. 3, line 60 - col. 4, line 4). Tanaka does not appear to teach that such a groove is positioned between a drain region and a gate dielectric layer or between a source region and a gate dielectric layer. As a result, one of ordinary skill would have no motivation to combine Tanaka with Maruo as suggested by the Examiner. Accordingly, applicant respectfully requests that the rejection be withdrawn. Claims 7-8 depend from claim 6, and for at least the same reasons as claim 6, applicant respectfully requests that the rejection of claims 7-8 be withdrawn.

Claims 9-12 were rejected under 35 U.S.C. 103(a) as unpatentable over Maruo in combination with Tanaka and U.S. Patent No. 5,989,963 to Luning et al. The rejection is respectfully traversed. Claims 9-12 depend from claim 6, which was discussed above. Applicant respectfully submits that the Examiner's citation of Luning et al. does not overcome the deficiencies as explained above for claim 6. In addition, applicant notes that the Examiner does not appear to have cited any portion of Luning that describes forming a screen oxide layer over "side surfaces" of a "recessed section" and "wherein the implanting including implanting through the side surfaces and the bottom surfaces" as recited in claim 9. Claims 10-11 depend from claim 9. Accordingly, for at least the same reasons as claim 6 and the reasons set forth above, applicant respectfully requests that the rejection of claims 9-12 be withdrawn.

Claims 13-15 were rejected under 35 U.S.C. 103(a) as unpatentable over Maruo in combination with Tanaka. The rejection is respectfully traversed. Claims 13-15 depend from claim 6 and the explanation above for claim 6 also applies to claims 13-15. In addition, applicant notes that the Examiner did not appear to cite any specific portion of the art describing or suggesting a method wherein "the first recessed section and the second recessed section each are formed in a tapered configuration" as recited in claim 13. Claims 14-15 depend from claim 13. Accordingly, for at least the same reasons as claim 6 and the reasons set forth above, applicant respectfully requests that the rejection of claims 13-15 be withdrawn.

Claim 16 was indicated as being allowable if rewritten in independent form. Applicant has done so and respectfully submits that claim 16 is in allowable form.

New dependent claims 21-30 have been added. Support for the claims may be found throughout the specification and figures and in the original claims. Examination is respectfully requested.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 6-16 and 21-30 are in patentable form for at least the reasons stated above. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES VICTOR & MANN, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212
Customer No. 24033

Dated: February 13, 2003

(310) 556-7983 (tele general)
(310) 871-8448 (tele direct)
(310) 556-7984 (facsimile)

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on February 13, 2003.

Alan S. Raynes

Alan S. Raynes **Feb. 13, 2003**
(Date)

Version With Markings to Show Changes Made

The paragraph at page 1, lines 6-9 was amended as follows:

Applicants hereby incorporate by reference Japanese Application No. 2000-132339, filed May 1, 2000 in its entirety. Applicants hereby incorporate by reference U.S. Application Serial No. 09/847,071 [_____, filed May 1, 2001, invented by Tatsuru Namatame and Kenji Yokoyama, having docket number 15.42/5850,] in its entirety.

Claims 6, 9, 14 and 16 were amended as follows:

6. (amended) A method for manufacturing a semiconductor device comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed;

implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section.

9. (amended) A method for manufacturing a semiconductor device according to claim 7, wherein the substrate includes side surfaces and a bottom surface in each of the first recessed section and the second recessed section and further comprising[,];

before the forming of the anti-oxidation layer, forming a protection film to cover the side surfaces and the bottom surface of semiconductor substrate in the first recessed section and in the

second recessed section; and

wherein the implanting includes implanting through the side surfaces and the bottom surfaces.

14. (amended) A method for manufacturing a semiconductor device according to claim 13, wherein a tapered angle of each of the first recessed section and the second recessed section is 60 degrees or greater and less than 90 degrees.

16. (amended) A method for manufacturing a semiconductor device [according to claim 15,] comprising a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer, the method comprising:

forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed;

implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section; and

thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section;

wherein the implanting direction of the impurity and the normal line of the surface of the semiconductor substrate during the implanting an impurity in the semiconductor substrate in the first recessed section and in the second recessed section defines an angle that is greater than zero degrees and no greater than 45 degrees.